What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a first conductivity type;

a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;

a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;

a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well;

a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well;

a heavily doped region of buried layer having the second conductivity type formed at a portion corresponding to the

first contact region in the first well; and

a heavily doped region of buried layer having the first conductivity type formed at a portion corresponding to the second contact region in the second well.

2. The semiconductor device as claimed in claim 1, wherein the heavily doped regions of buried layers having the first and second conductivity types are spaced at a distance of about 0.25 to 1.0 μm beneath the major surface of the semiconductor substrate.

3. The semiconductor device as claimed in claim 1, wherein the junction depth of the first and second wells is 1.5 to 2.0 μm.

4. The semiconductor device as claimed in claim 1, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second

contact region.

5. The semiconductor device as claimed in claim 1, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

6. A method of fabricating a semiconductor device comprising the steps of:

forming a field oxide layer on a semiconductor substrate having a first conductivity type where the semiconductor substrate is included first and second MOS transistor regions and first and second contact regions;

forming a first well having a second conductivity type in the major surface of the semiconductor substrate having the first MOS transistor region and the first contact region;

forming a heavily doped region of buried layer having the second conductivity type at a portion spaced corresponding to

the first contact region in the first well;

forming a second well having the first conductivity type in the semiconductor substrate having the second MOS transistor region and the second contact region; and

forming a heavily doped region of buried layer having the first conductivity type at a portion spaced corresponding to the second contact region in the second well.

7. The method as claimed in claim 6, wherein the heavily doped region of buried layer having the first and second conductivity types are spaced at a distance of about 0.25 to 1.0 μm beneath the major surface of the semiconductor substrate.

8. The method as claimed in claim 6, wherein the junction depth of the first and second wells is 1.5 to 2.0 μm.

9. The method as claimed in claim 6, wherein the concentration of the heavily doped region of buried layer

having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

10. The method as claimed in claim 6, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

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